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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Stefan Hau-Riege
R. Scott List

Serial No.: 10/001,305

Filed: November 30, 2001

For: METHOD OF MAKING A SEMICONDUCTOR DEVICE THAT HAS COPPER DAMASCENE INTERCONNECTS WITH ENHANCED ELECTROMIGRATION RELIABILITY

Art Unit: 2829

Examiner: M. Harrison

Atty Docket: P12075

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF R. SCOTT LIST UNDER 37 C.F.R. § 1.131

Dear Sir:

I, R. Scott List, declare that:

1. I am an inventor of the subject matter claimed in the captioned non-provisional patent application.

2. No later than April 2001, I and co-inventor Stefan Hau-Riege submitted to the Intel legal department an invention disclosure that described a method for improving interconnect electromigration reliability through local doping of the interconnect. That invention disclosure described and illustrated two techniques for performing such a local doping operation. The first technique (illustrated by figures 3(a) -3(c) of the invention disclosure at page 9) comprised forming a conductive layer on a substrate, forming a dielectric layer on the conductive layer, etching a via through the dielectric layer to expose part of the conductive layer, then introducing a dopant into

that exposed part of that layer. The second technique (illustrated by figures 4(a) -4(b) of the invention disclosure at page 10) comprised forming a dielectric layer on a substrate, etching the dielectric layer to form a via and trench, filling the via and trench with a conductive layer, exposing part of the conductive layer, then introducing a dopant into that exposed part of that layer. Attached as Exhibit A is a true and correct copy of that invention disclosure, which was sent to the Intel legal department no later than April, 2001.

3. In May 2001, I was informed that a patent application would be filed for the invention that is described in Exhibit A.

4. After receiving and reviewing a draft patent application that accurately and completely described my invention, I signed a Declaration and Power of Attorney form and an assignment for the patent application, which were sent to Mark V. Seeley, the patent attorney who drafted the patent application.

5. I understand that this declaration is being submitted to support a response to an Office Action mailed on December 9, 2003 for U.S. Patent Application Serial Number 10/001,305 entitled "Method of Making a Semiconductor Device that has Copper Damascene Interconnects with Enhanced Electromigration Reliability."

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the captioned application or any patent issued thereon.

Date: 1/9/04

R. Scott List

R. Scott List

INTEL CONFIDENTIAL
Attorney-Client Privileged Communication

#1

18884
TMG/Process Comm / TMG/CR

TMG INVENTION DISCLOSURE, R v 3, 8/99

Located at: http://legal.intel.com

APR 12 2001

LEGAL ID# _____(legal dept. use only) DATE: _____

It is important to provide accurate and detailed information on this form (fill in ALL areas under Inventor[s]). The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to **Janice Boulden, Intel Legal Department at JF3-147. You can submit electronically if all of the information is electronic, including drawings and supervisor approval.** If you have any questions regarding this form or to whom it should be forwarded, please call **503-264-0444**.

Fill out the below and follow the instructions:

1. Field of the Invention:

- [X] **Semiconductor Process: device and integration**
- [ ] **Semiconductor Process + Equipment: thin films**
- [ ] **Semiconductor Process + Equipment: etch/litho**
- [ ] **Circuit Design**
- [ ] **Flash**
- [ ] **Test**
- [ ] **CQN (Q&R)**
- [ ] **Packaging**
- [ ] **Boards/Cartridge**
- [ ] **Automation**
- [ ] **Other**

2. Concise Title of Invention:

Electromigration Reliability Improvement In Cu Damascene Interconnects With Minimal Resistance Impact Through Localized Doping and Method of Making The Same

3. **Brief Description of Inventi n (pleas us only spac provided and font #10 or larger. Write the K y Elements of the Inv ntion):**

Th invention is:

A methodology for improving interconnect electromigration reliability through local doping of the interconnect material (existing doping techniques dope the entire line). Local doping slows electromigration near vias and contacts, which are the areas of primary reliability concern, while minimizing the electrical resistance impact, since the bulk of the line is undoped and therefore does not suffer a resistance increase. This invention also describes several alternative process flows to achieve local doping.

The key elements are:

1. Local doping of the interconnect material near vias and contacts.

2. Integration schemes for local doping with lowest cost impact:

(a) No additional mask required for worst-case enclosure ("via-above", Fig. 1) structures. Process is self-aligned by using the via openings as masking layer. Local doping can be achieved by the following methods:

(i) Deposit dopant layer after nitride breakthrough but prior to barrier/seed deposition. An annealing step drives the dopant into the metal. Optionally, remove the dopant layer after the drive in of the dopant.
(ii) Ion-implant the dopant after nitride breakthrough and drive-in anneal.
(iii) Selectively deposit dopant through CVD or electroless deposition and drive-in anneal.

(b) (Optional) For locally doping the intrinsically more reliable coverage ("via above", Fig. 2) structures, one mask per metal layer is required, because the process is not self-aligned. Local doping of coverage structures be omitted since the lifetimes of coverage structures is generally twice as large as the lifetime of enclosure structures.

3. The resistance impact can be comprehended in design tools by considering an increased via or contact resistance.

4. Inventor(s):

Name: Stefan Hau-Riege
E-Mail Address: stefan.p.hau-riege@intel.com WWID#10637121 M/S: RA1-240

Phone: 613-6935 Fax:613-8963 Home Address:19520 NW Decora Lane #1133, Hillsboro, OR 97124

Citizenship: German
Supervisor Name: Scott List
Supervisor Phone: 613-4826
Supervisor M/S:RA1-204
Group Name: TMG
Contractor:
Inventor Signature:
Division Name: ATD___
PTD___ CTM___ CR_X_
YES _____
STTD___ CQN ___
SMTD___TCAD___
NO ____X___
Oth r?_____

Name: Scott List

E-Mail Address: scott.list@intel.com WWID#10582769 M/S: RA1-204

Phone: 613-4826 Fax:613-8963 Home Address:16675 SW Ivy Glenn Street Beaverton, OR 97007

Citizenship: USA
Supervisor Name: Jerry Marcyk
Supervisor Phone:613-6662
Supervisor M/S:RA1-234
Group Name: TMG
Contractor:
Inventor Signature: N. Scott List
Division Name: ATD___
PTD___ CTM___ CR_X_
YES _____
STTD___ CQN ___
SMTD___TCAD___
NO _____
Other?_____

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

5. **HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (us first inv nt r's supervisor if multiple inv nt rs)**

DATE: 3/28/01 **SUPERVISOR NAME:** M. Scott Duf

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

6. **Has subject matter of present disclosure been disclosed or will it be disclosed outside Intel? No**
If yes, explain and give date:
(Give expected tape out date if applicable):

7. **Has the subject matter of present disclosure been published or will it be published outside of Intel? No**
If yes, explain and give date:

8. **Has a product using or manufactured using the present disclosure been sold or offered for sale?**
If yes, explain and give date: No

9. **Has this invention been conceived, or constructed during accomplishment of a government or third party contract? If yes, give contract name and number: No**

10. **Explain the problem being addressed by the invention:**

This invention addresses the problem of:
A major reliability concern in today's integrated circuits is failure of metallic interconnect mainly due to electromigration. Electromigration imposes limits on the maximum allowed currents in interconnects. Interconnect reliability can be enhanced through doping of the interconnect, which retards electromigration by slowing metal diffusion.

11. **Explain current state of the art (i.e, how the problem is solved today):**

Presently the problem described above is solved by:
Presently, certain metal levels are doped globally to slow electromigration by using methods such as doped seeds, co-plating, co-sputtering, or ion-implantation of dopants. Since the whole interconnect is doped (including large parts which are not prone to electromigration-induced failure), the associated resistance increase is substantial. To reduce RC delay, the amount of doping has to be minimized, or, for speed-critical layers, the metal has to stay undoped.

12. **Explain technical advantages of the invention over current state of the art:**

The technical advantage of this invention is:
To obtain similar or better reliability improvement with less resistance increase than global doping. Local doping can exceed doping levels used for global doping.

13. a. **Is the invention experimentally verified?** No
b. **Is the invention verified with simulation?** Yes
c. **If neither a. or b. above, then you can get a patent on the concept, but please explain the technical basis to justify that your invention will work (use extra space if necessary):**

14. Detailed Description f Inv nti n (try t use only the space provided with f nt #10 or larg r type. Refer t your drawings):

Introduction

Electromigration-induced voiding in Cu-based interconnects occurs primarily near the cathode via at the Cu/SiN interface, and eventually leads to open-circuit failure. Unlike voids in Al-based metallization schemes, voids in Cu-based metallization schemes are typically shallow and are located along the Cu/SiN interface. The enclosure structures, shown in Fig. 1, are the worst-case structures with regard to electromigration. Interconnect failure is induced by a void which nucleated near the cathode via and which has grown to expose the bottom of the via above. The coverage structure, shown in Fig. 2, is intrinsically more reliable than the enclosure structure, because the void has to grow from the top surface, which is the void nucleation site, to the bottom via. The reliability of Cu interconnects is improved through the incorporation of dopants which retard electromigration, but the dopant concentration is bound by maximum allowed resistance increase associated with doping.

Structure

The primary reliability concern is the part of the interconnect system which is connected through vias or contacts to other metal layers or silicon (poly or diffusion). This invention is to improve electromigration resistance at these sites through locally doping interconnects near vias and contacts. Local doping will slow void nucleation and growth in areas where voiding can lead to catastrophic failure quickly. Instead, voids will nucleate and grow in less critical areas downstream of the vias and contacts. Because the doping is local and only leads to a small resistance increase, local doping levels can exceed the doping levels used for global doping,

Materials

The dopant has to effectively retard electromigration with minimal electrical resistance increase. The dopant should also diffuse into the copper to some extent to protect a larger area around a via/contact, and to ensure a somewhat diffuse dopant profile in order to prevent a new flux divergence site which could lead to failure. It is also preferable for the dopant to not diffuse into the ILD. Preferred materials include (but is not limited to) Al, Cd, Mg, Sn, and Zr.

Process

For cost considerations, the goal is to incorporate local doping into the backend interconnect process with a minimum number of masks and process steps. We suggest several process options which facilitate local interconnect doping. For the more-critical enclosure structures, no extra mask set is required because the process is self-aligned through via cuts. For the less critical coverage structures, one additional mask is required. If the latter option is chosen, the process flow for coverage structures would be able to cover both the enclosure and coverage case. The process flows are summarized in Table (I) and are illustrated in Figures (3) and (4)

(A) Enclosure Structures (Table I (A) and Fig. 3):

One option is to deposit a dopant layer after nitride breakthrough and drive the doping material into the Cu through a subsequent annealing step. The dopant layer can either be kept (option (i), Fig. 3(a)) or removed (option (ii), Fig. 3(b)). Alternatively, dopants can be incorporated after the nitride breakthrough through ion implantation or gas exposures (e.g., exposure to silane) (option (iii), Fig. 3(b)), or dopant layers can be deposited selectively into via cuts (option (iv), Fig. 3(c)). In both cases, an optional anneal or the high temperatures during subsequent process steps will drive the dopant into the Cu.

(B) Coverage Structures (Table I (B) and Fig. 4):

Either photoresist is used to define the areas of the interconnect which will receive local doping (options (i) and (ii)), or a thin, patterned SiN/SiC layer can serve this purpose (options (iii) and (iv)). The dopants are incorporated either through ion implantation or gas exposures (e.g., exposure to silane) (options (i) and (iii)) or a dopant layer is selectively deposited onto the exposed Cu (options (ii) and (iv)). Again, in all cases, an optional anneal or the high temperatures during subsequent process steps will drive the dopant into the Cu.

Ref renced sketch s/dwg's/diagrams: (us additional page(s))

15.

Drawings (us as many pages as needed)
(PLEASE DO NOT MAKE COLOR DRAWINGS)

Figure 1. Present State f th Art (often this is h lpful to xplain your invention, but it is not required).

Figure are attached to end of form.

Figure 2&3. The Invention (use additional figures as needed to show details and additional embodiments)

Figure are attached to end of form.

16. **Key Supporting Data (1 page limit on separate page):**

17. **What is the product or process invention to be used on? (e.g., P8xx, name of product, etc.): P1264 and beyond**

18. **Have you reviewed your invention with a TMG Patent Mentor? (see below for mentor names) If so, give name: __Ken Cadien_____**

19. **Any other information IP committee should consider?**

MENTOR REVIEW

If you don't already have a departmental peer review process for invention disclosures, we recommend you have it reviewed by a Mentor before you send your invention disclosure to Intel Legal. The purpose of this Mentor review is to ensure that the invention disclosure is written clearly enough for the IP Committee to comprehend your invention including all the novel aspects of it. Please refer to the list below for recommended Mentors by area. Select ONE Mentor to review and acknowledge. This recommended step is not meant to unreasonably slow down the invention disclosure process. If your Mentor fails to respond to you in a reasonable amount of time, then send your invention disclosure directly to Intel Legal.

Area	Mentor
Semic nductor Process – device and integration	Mark Bohr, Robert Chau, Krishna Seshan
Semiconductor Process – thin films	Ken Cadien, Chien Chiang, John Carruthers

Semiconductor Process – etch/litho	John Carruthers, Peter Silverman, Peter Charvat (etch), Yan Borodovsky (litho)
Circuit Design	Ian Young, Greg Taylor, Clair Webb, Rajesh Galivanch
Flash	Manzur Gill, Krishna Seshan
Test	J.J. Grealish, Rajesh Galivanche, Mike Mayberry
CQN (Q&R)	Ian Young, Greg Taylor, Clair Webb, John Carruthers, Valluri (Bob) Rao, Naomi Obinata
Packaging	Ken Kinsman, Bob Sankman, Rama Shukula
Boards/Cartridge	Leslie Polaski, J.J. Grealish
Automation	Sunit Rikhi
Optical and MEMS	Valluri (Bob) Rao
Legal Dept. Patent Attorneys	Ray Werner, Rob Winkle, Naomi Obinata, John Greaves

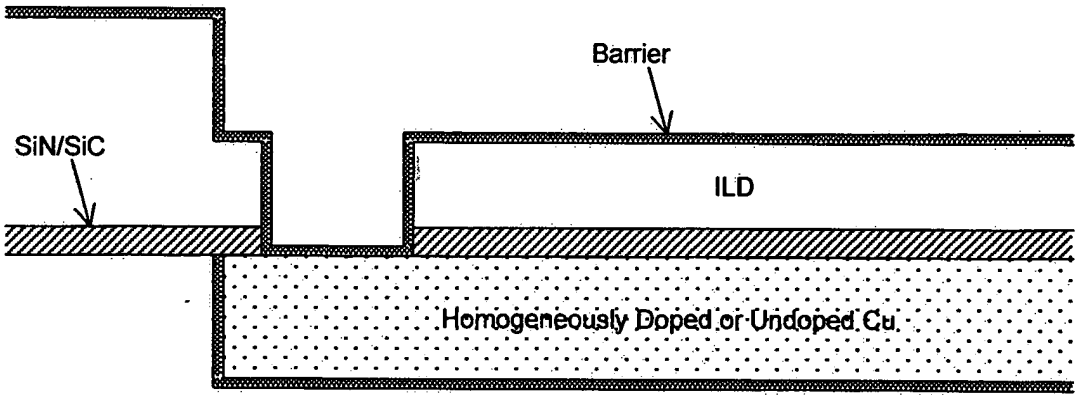

Figure 1 (Present State of the Art)

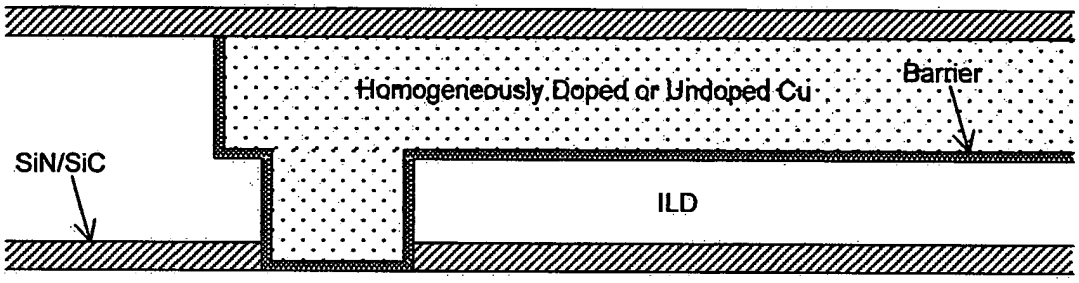

Figure 2 (Present State of the Art)

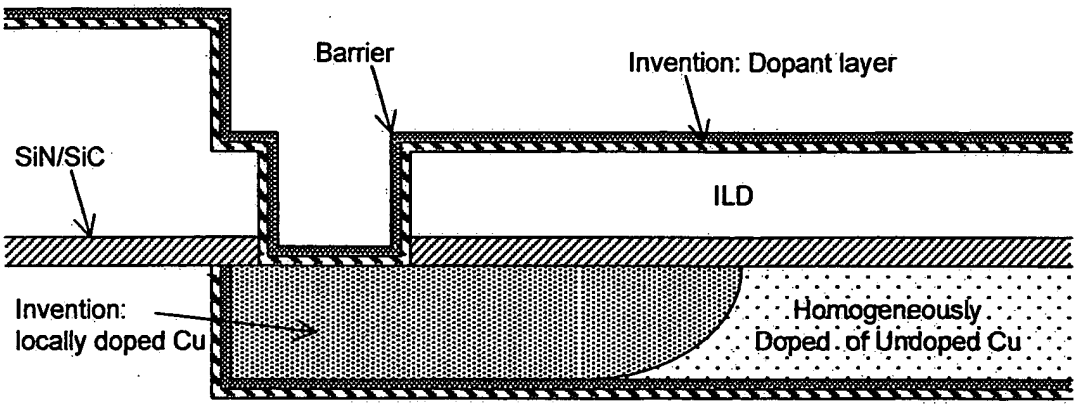

Figure 3 (a) (The Invention)

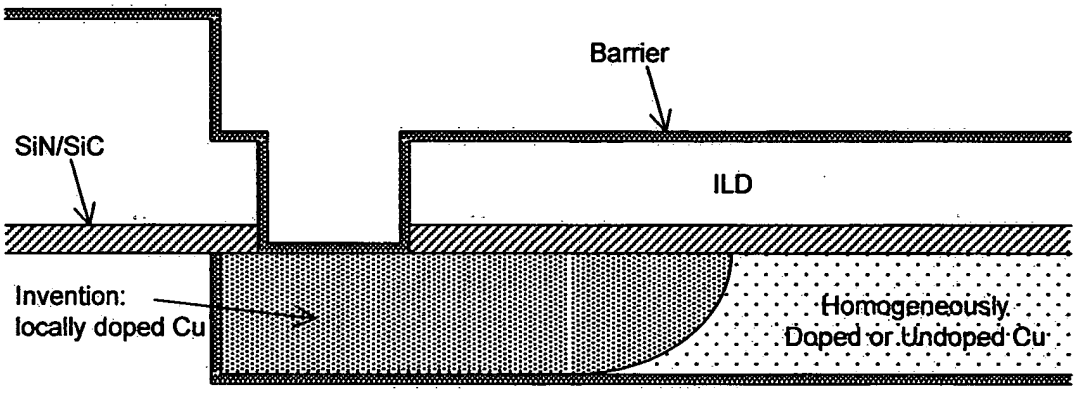

Figure 3 (b) (The Invention)

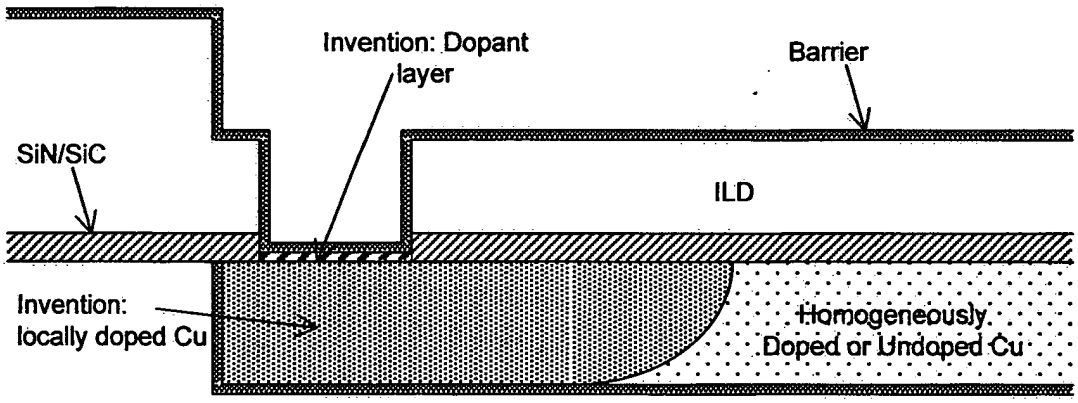

Figure 3 (c) (The Invention)

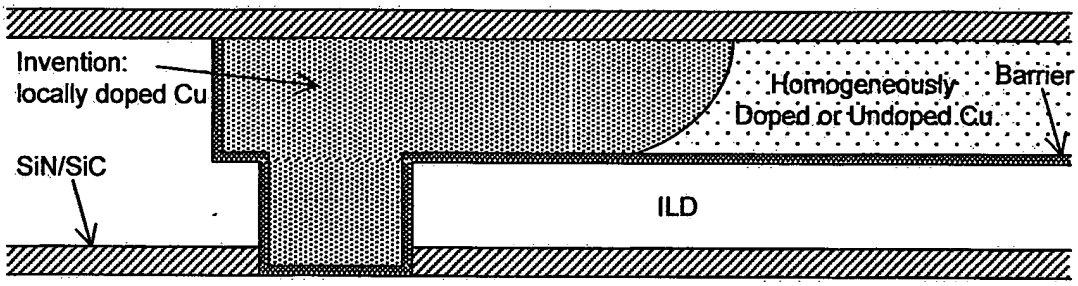

Figure 4 (a) (The Invention)

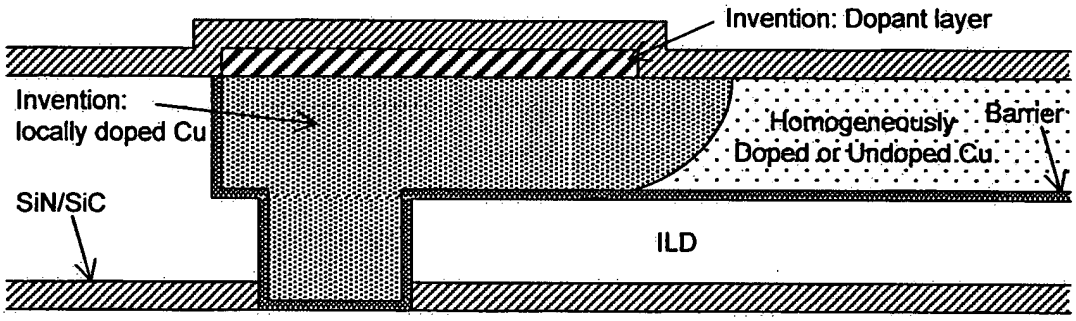

Figure 4 (b) (The Invention)

Table I: Possible Process Flows

(A) Enclosure (Fig. 1): Insert process steps after nitride breakthrough but before barrier/seed deposition. No mask required because process if self-aligned. Several process options (i) – (iv):

(i) Fig. 3 (a)
  (1) Deposit thin, continuous dopant layer
  (2) Drive-in anneal (optional)
  (dopant layer will be removed by subsequent CMP step)

(ii) Fig. 3 (b)
  (1) Deposit thin, continuous dopant layer
  (2) Drive-in anneal (optional)
  (3) Remove dopant layer through wet or dry etching

(iii) Fig. 3 (b) – Implant version
  (1) Ion-implant dopant
  (2) Drive-in anneal

(iv) Fig. 3 (c)
  (1) Selectively deposit dopant layer on Cu
  (2) Drive-in anneal (optional)

(B) Optional treatment for coverage structures (Fig. 2): Insert process steps after nitride breakthrough but before barrier/seed deposition. One mask required. Several process options (i) – (iv):

(i) Fig. 4 (a) – photoresist as doping mask
  (1) Pattern photoresist to leave openings over interconnects with vias underneath
  (2) Selectively deposit dopant layer
  (3) Remove photoresist using a Cu-inert chemical
  (4) Drive-in anneal

(ii) Fig. 4 (b) – photoresist as doping mask
  (1) Pattern photoresist to leave openings over interconnects with vias underneath
  (2) Ion-implant dopant
  (3) Remove photoresist using a Cu-inert chemical
  (4) Drive-in anneal

(iii) Fig. 4 (a) – SiN/SiC as doping mask
  (1) Deposit thin SiN/SiC layer
  (2) Pattern photoresist to leave openings over interconnects with vias underneath
  (3) Etch SiN/SiC, remove PR
  (4) Selectively deposit dopant layer
  (5) Drive-in anneal

(iv) Fig. 4 (b) – SiN/SiC as doping mask
  (1) Deposit thin SiN/SiC layer
  (2) Pattern photoresist to leave openings over interconnects with vias underneath
  (3) Etch SiN/SiC, remove PR
  (4) Ion-implant dopant
  (5) Drive-in anneal

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Stefan Hau-Riege
R. Scott List

Serial No.: 10/001,305

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For: METHOD OF MAKING A SEMICONDUCTOR DEVICE THAT HAS COPPER DAMASCENE INTERCONNECTS WITH ENHANCED ELECTROMIGRATION RELIABILITY

Art Unit: 2829

Examiner: M. Harrison

Atty Docket: P12075

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF MARK V. SEELEY
UNDER 37 C.F.R. § 1.131

Dear Sir:

I, Mark V. Seeley, declare that:

1. I am a patent attorney with Intel Corporation, the assignee of the captioned non-provisional patent application, which I drafted.

2. In April 2001, the Intel legal department received an invention disclosure that described a method for improving interconnect electromigration reliability through local doping of the interconnect. That invention disclosure described and illustrated two techniques for performing such a local doping operation. The first technique (illustrated by figures 3(a) -3(c) of the invention disclosure at page 9) comprised forming a conductive layer on a substrate, forming a dielectric layer on the conductive layer, etching a via through the dielectric layer to expose part of the conductive layer, then introducing a dopant into that exposed part of that layer. The second technique (illustrated by figures 4(a) -4(b) of the invention

disclosure at page 10) comprised forming a dielectric layer on a substrate, etching the dielectric layer to form a via and trench, filling the via and trench with a conductive layer, exposing part of the conductive layer, then introducing a dopant into that exposed part of that layer. Attached as Exhibit A is a true and correct copy of that invention disclosure, showing date stamps of April 12, 2001 and April 17, 2001.

3. The invention disclosure was assigned to an Intel invention review committee for evaluation. The committee met to review that invention disclosure, along with many others, on May 22, 2001. At that time, the committee chose to file a patent application for the invention described in the above referenced invention disclosure. I understand the application was assigned to me for drafting on June 1, 2001.

4. After receiving the file, I generated an initial draft of a patent application for the invention described in the invention disclosure. As is my usual practice, I completed the initial draft prior to discussing the invention with either of the inventors. I did not retain a copy of that initial draft.

5. I believe I revised the application after obtaining inventor feedback on the initial draft, and forwarded the revised draft to the inventors for review.

6. I understand the inventors, Messrs. List and Hau-Reige, concluded that the latest revised draft accurately and completely described their invention. They then signed Declaration and Power of Attorney forms for the application, and assignments for it, and returned those documents to me. Attached as Exhibit B is a true and correct copy of the Declaration and Power of Attorney, which Mr. Hau-Reige returned, that he signed on November 17, 2001. Attached as Exhibit C is a true and correct copy of the assignment, which Mr. Hau-Reige returned, that he signed, also on November 17, 2001. Attached as Exhibit D is a true and correct copy of the Declaration and Power of Attorney, which Mr. List returned, that he signed on November 27, 2001. Attached as Exhibit E is a true and correct copy of the assignment, which Mr. List returned, that he signed, also on November 27, 2001.

7. I drafted an information disclosure statement for the application, which I signed on November 30, 2001. Attached as Exhibit F is a true and correct copy of that information disclosure statement. After receiving the Declaration and Power of Attorney forms and the assignments, I had the patent application filed on November 30, 2001.

8. This declaration is being submitted to support a response to an Office Action mailed on December 9, 2003 for U.S. Patent Application Serial Number 10/001,305 entitled "Method of Making a Semiconductor Device that has Copper Damascene Interconnects with Enhanced Electromigration Reliability."

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the captioned application or any patent issued thereon.

Date: January 14, 2004

Mark V. Seeley

INTEL CONFIDENTIAL
Attorney-Client Privileged Communication

#1

18884
TMG/Process Comm/TMG/cR

TMG INVENTION DISCLOSURE, R v 3, 8/99

Located at: http://legal.intel.com

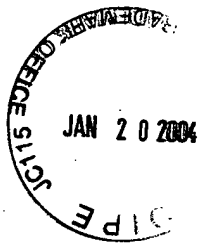
APR 12 2001

LEGAL ID# _____(legal dept. use only) DATE: _____

It is important to provide accurate and detailed information on this form (fill in ALL areas under Inventor[s]). The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to **Janice Boulden, Intel Legal Department at JF3-147. You can submit electronically if all of the information is electronic, including drawings and supervisor approval.** If you have any questions regarding this form or to whom it should be forwarded, please call **503-264-0444**.

Fill out the below and follow the instructions:

1. Field of the Invention:



- X **Semiconductor Process: device and integration**
- ☐ **Semiconductor Process + Equipment: thin films**
- ☐ **Semiconductor Process + Equipment: etch/litho**
- ☐ **Circuit Design**
- ☐ **Flash**
- ☐ **Test**
- ☐ **CQN (Q&R)**
- ☐ **Packaging**
- ☐ **Boards/Cartridge**
- ☐ **Automation**
- ☐ **Other**

2. Concise Title of Invention:

Electromigration Reliability Improvement In Cu Damascene Interconnects With Minimal Resistance Impact Through Localized Doping and Method of Making The Same

3. **Brief Description of Invention (please use only space provided and font #10 or larger. Write th Key Elements of the Inv ntion):**

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The key elements are:

1. Local doping of the interconnect material near vias and contacts.

2. Integration schemes for local doping with lowest cost impact:

(a) No additional mask required for worst-case enclosure ("via-above", Fig. 1) structures. Process is self-aligned by using the via openings as masking layer. Local doping can be achieved by the following methods:

(i) Deposit dopant layer after nitride breakthrough but prior to barrier/seed deposition. An annealing step drives the dopant into the metal. Optionally, remove the dopant layer after the drive in of the dopant.
(ii) Ion-implant the dopant after nitride breakthrough and drive-in anneal.
(iii) Selectively deposit dopant through CVD or electroless deposition and drive-in anneal.

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3. The resistance impact can be comprehended in design tools by considering an increased via or contact resistance.

4. Inventor(s):

Name: Stefan Hau-Riege
E-Mail Address: stefan.p.hau-riege@intel.com WWID#10637121 M/S: RA1-240

Phone: 613-6935 Fax:613-8963 Home Address:19520 NW Decora Lane #1133, Hillsboro, OR 97124

Citizenship: German
Group Name: TMG
Division Name: ATD___
PTD___ CTM___ CR_X_
STTD___ CQN ___
SMTD___TCAD___
Other?_____

Supervisor Name: Scott List
Contractor:
YES _____
NO ____X___

Supervisor Phone: 613-4826
Inventor Signature:

Supervisor M/S:RA1-204

Name : Scott List

E-Mail Address: scott.list@intel.com WWID#10582769 M/S: RA1-204

Phone: 613-4826 Fax:613-8963 Home Address:16675 SW Ivy Glenn Street Beaverton, OR 97007

Citizenship: USA
Group Name: TMG
Division Name: ATD___
PTD___ CTM___ CR_X_
STTD___ CQN ___
SMTD___TCAD___
Other?_____

Supervisor Name: Jerry Marcyk
Contractor:
YES _____
NO _____

Supervisor Phone:613-6662
Inventor Signature: N. Scott List

Supervisor M/S:RA1-234

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

5. **HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (us first inv nt r's supervis r if multiple inventors)**

DATE: 3/28/01 **SUPERVISOR NAME:** M. Pelt-Dyl

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

6. **Has subject matter of present disclosure been disclosed or will it be disclosed outside Intel? No**
If yes, explain and give date:
(Give expected tape out date if applicable):

7. **Has the subject matter of present disclosure been published or will it be published outside of Intel? No**
If yes, explain and give date:

8. **Has a product using or manufactured using the present disclosure been sold or offered for sale?**
If yes, explain and give date: No

9. **Has this invention been conceived, or constructed during accomplishment of a government or third party contract? If yes, give contract name and number: No**

10. **Explain the problem being addressed by the invention:**

This invention addresses the problem of:
A major reliability concern in today's integrated circuits is failure of metallic interconnect mainly due to electromigration. Electromigration imposes limits on the maximum allowed currents in interconnects. Interconnect reliability can be enhanced through doping of the interconnect, which retards electromigration by slowing metal diffusion.

11. **Explain current state of the art (i.e, how the problem is solved today):**

Presently the problem described above is solved by:
Presently, certain metal levels are doped globally to slow electromigration by using methods such as doped seeds, co-plating, co-sputtering, or ion-implantation of dopants. Since the whole interconnect is doped (including large parts which are not prone to electromigration-induced failure), the associated resistance increase is substantial. To reduce RC delay, the amount of doping has to be minimized, or, for speed-critical layers, the metal has to stay undoped.

12. **Explain technical advantages of the invention over current state of the art:**

The technical advantage of this invention is:
To obtain similar or better reliability improvement with less resistance increase than global doping. Local doping can exceed doping levels used for global doping.

13. a. **Is the invention experimentally verified?** No
b. **Is the invention verified with simulation?** Yes
c. **If neither a. or b. above, then you can get a patent on the concept, but please explain the technical basis t justify that your invention will work (use xtra spac if n cessary):**

14. Detailed Description of Inv ntion (try to use only the space provided with font #10 or larger type. Refer to your drawings):

Introducti n

Electromigration-induced voiding in Cu-based interconnects occurs primarily near the cathode via at the Cu/SiN interface, and eventually leads to open-circuit failure. Unlike voids in Al-based metallization schemes, voids in Cu-based metallization schemes are typically shallow and are located along the Cu/SiN interface. The enclosure structures, shown in Fig. 1, are the worst-case structures with regard to electromigration. Interconnect failure is induced by a void which nucleated near the cathode via and which has grown to expose the bottom of the via above. The coverage structure, shown in Fig. 2, is intrinsically more reliable than the enclosure structure, because the void has to grow from the top surface, which is the void nucleation site, to the bottom via. The reliability of Cu interconnects is improved through the incorporation of dopants which retard electromigration, but the dopant concentration is bound by maximum allowed resistance increase associated with doping.

Structure

The primary reliability concern is the part of the interconnect system which is connected through vias or contacts to other metal layers or silicon (poly or diffusion). This invention is to improve electromigration resistance at these sites through locally doping interconnects near vias and contacts. Local doping will slow void nucleation and growth in areas where voiding can lead to catastrophic failure quickly. Instead, voids will nucleate and grow in less critical areas downstream of the vias and contacts. Because the doping is local and only leads to a small resistance increase, local doping levels can exceed the doping levels used for global doping,

Materials

The dopant has to effectively retard electromigration with minimal electrical resistance increase. The dopant should also diffuse into the copper to some extent to protect a larger area around a via/contact, and to ensure a somewhat diffuse dopant profile in order to prevent a new flux divergence site which could lead to failure. It is also preferable for the dopant to not diffuse into the ILD. Preferred materials include (but is not limited to) Al, Cd, Mg, Sn, and Zr.

Process

For cost considerations, the goal is to incorporate local doping into the backend interconnect process with a minimum number of masks and process steps. We suggest several process options which facilitate local interconnect doping. For the more-critical enclosure structures, no extra mask set is required because the process is self-aligned through via cuts. For the less critical coverage structures, one additional mask is required. If the latter option is chosen, the process flow for coverage structures would be able to cover both the enclosure and coverage case. The process flows are summarized in Table (I) and are illustrated in Figures (3) and (4)

(A) Enclosure Structures (Table I (A) and Fig. 3):

One option is to deposit a dopant layer after nitride breakthrough and drive the doping material into the Cu through a subsequent annealing step. The dopant layer can either be kept (option (i), Fig. 3(a)) or removed (option (ii), Fig. 3(b)). Alternatively, dopants can be incorporated after the nitride breakthrough through ion implantation or gas exposures (e.g., exposure to silane) (option (iii), Fig. 3(b)), or dopant layers can be deposited selectively into via cuts (option (iv), Fig. 3(c)). In both cases, an optional anneal or the high temperatures during subsequent process steps will drive the dopant into the Cu.

(B) Coverage Structures (Table I (B) and Fig. 4):

Either photoresist is used to define the areas of the interconnect which will receive local doping (options (i) and (ii)), or a thin, patterned SiN/SiC layer can serve this purpose (options (iii) and (iv)). The dopants are incorporated either through ion implantation or gas exposures (e.g., exposure to silane) (options (i) and (iii)) or a dopant layer is selectively deposited onto the exposed Cu (options (ii) and (iv)). Again, in all cases, an optional anneal or the high temperatures during subsequent process steps will drive the dopant into the Cu.

Referenced sk tches/dwg's/diagrams: (use additional page(s))

15.

Drawings (use as many pages as needed)
(PLEASE DO NOT MAKE COLOR DRAWINGS)

Figure 1. Present Stat of the Art (often this is helpful to explain your inventi n, but it is not required).

Figure are attached to end of form.

Figure 2&3. The Invention (use additional figures as needed to show details and additional embodiments)

Figure are attached to end of form.

16. Key Supporting Data (1 page limit on separate page):

17. What is the product or process invention to be used on? (e.g., P8xx, name of product, etc.):
P1264 and beyond

18. Have you reviewed your invention with a TMG Patent Mentor? (see below for mentor names) If so, give name: __Ken Cadien_____

19. Any other information IP committee should consider?

MENTOR REVIEW

If you don't already have a departmental peer review process for invention disclosures, we recommend you have it reviewed by a Mentor before you send your invention disclosure to Intel Legal. The purpose of this Mentor review is to ensure that the invention disclosure is written clearly enough for the IP Committee to comprehend your invention including all the novel aspects of it. Please refer to the list below for recommended Mentors by area. Select ONE Mentor to review and acknowledge. This recommended step is not meant to unreasonably slow down the invention disclosure process. If your Mentor fails to respond to you in a reasonable amount of time, then send your invention disclosure directly to Intel Legal.

Area	Mentor
Semiconductor Process – device and integration	Mark Bohr, Robert Chau, Krishna Seshan
Semiconductor Process – thin films	Ken Cadien, Chien Chiang, John Carruthers

Semiconductor Process – etch/litho	John Carruthers, Peter Silverman, Peter Charvat (etch), Yan Borodovsky (lith)
Circuit Design	Ian Young, Greg Taylor, Clair Webb, Rajesh Galivanche
Flash	Manzur Gill, Krishna Seshan
Test	J.J. Grealish, Rajesh Galivanche, Mike Mayberry
CQN (Q&R)	Ian Young, Greg Taylor, Clair Webb, John Carruthers, Valluri (Bob) Rao, Naomi Obinata
Packaging	Ken Kinsman, Bob Sankman, Rama Shukula
Boards/Cartridge	Leslie Polaski, J.J. Grealish
Automation	Sunit Rikhi
Optical and MEMS	Valluri (Bob) Rao
Legal Dept. Patent Attorneys	Ray Werner, Rob Winkle, Naomi Obinata, John Greaves

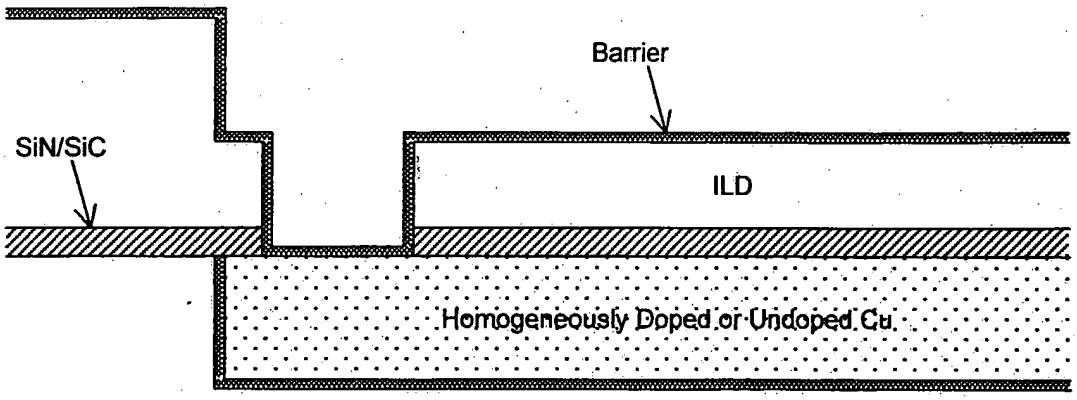

Figure 1 (Present State of the Art)

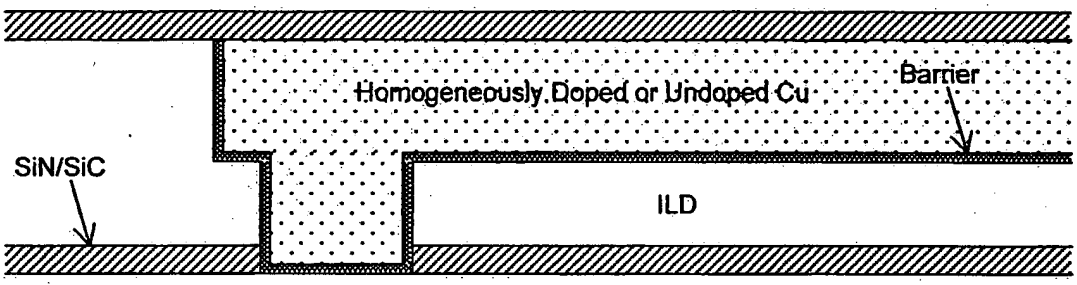

Figure 2 (Present State of the Art)

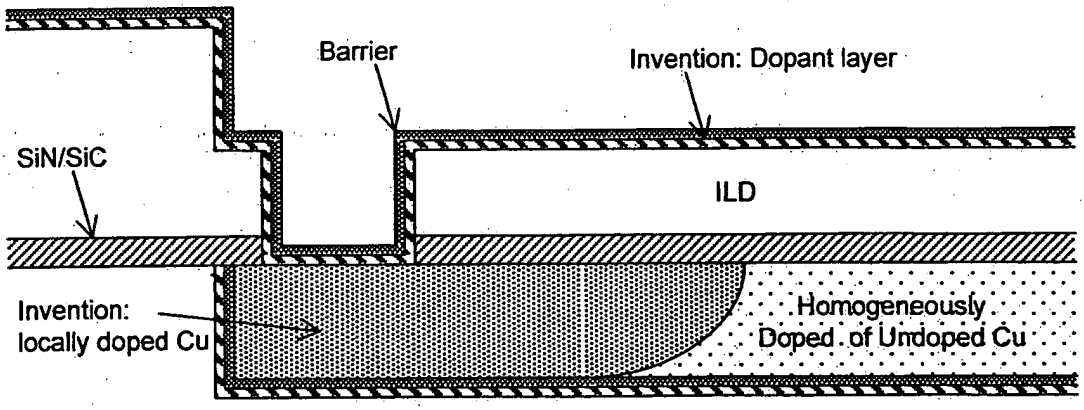

Figure 3 (a) (The Invention)

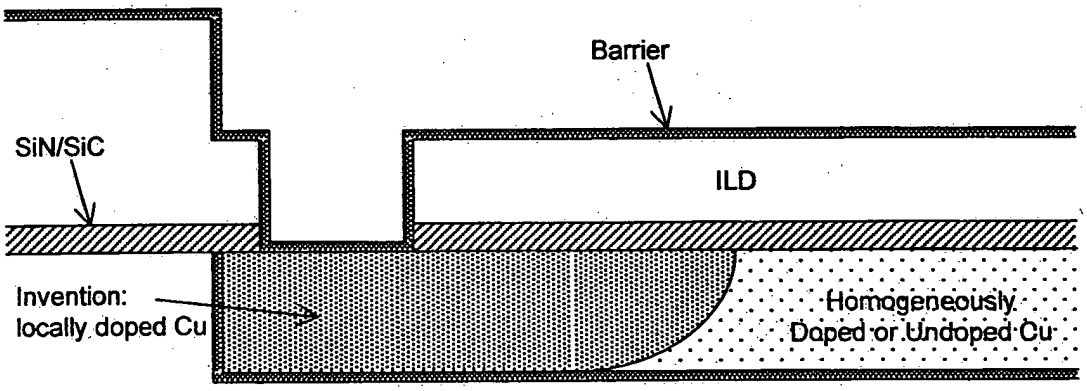

Figure 3 (b) (The Invention)

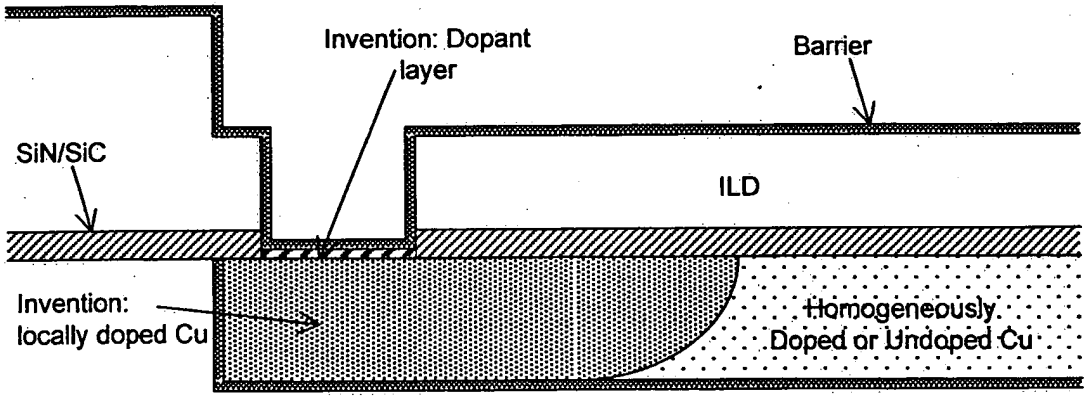

Figure 3 (c) (The Invention)

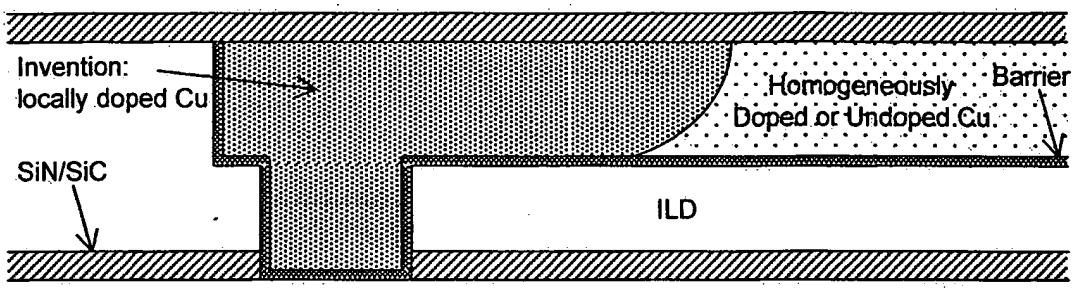

Figure 4 (a) (The Invention)

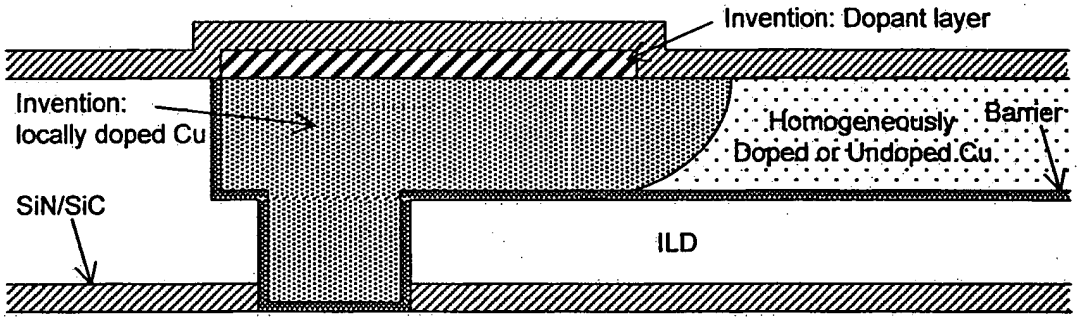

Figure 4 (b) (The Invention)

Table I: Possible Process Flows

(A) Enclosure (Fig. 1): Insert process steps after nitride breakthrough but before barrier/seed deposition. No mask required because process if self-aligned. Several process options (i) – (iv):

(i) Fig. 3 (a)
- (1) Deposit thin, continuous dopant layer
- (2) Drive-in anneal (optional)

(dopant layer will be removed by subsequent CMP step)

(ii) Fig. 3 (b)
- (1) Deposit thin, continuous dopant layer
- (2) Drive-in anneal (optional)
- (3) Remove dopant layer through wet or dry etching

(iii) Fig. 3 (b) – Implant version
- (1) Ion-implant dopant
- (2) Drive-in anneal

(iv) Fig. 3 (c)
- (1) Selectively deposit dopant layer on Cu
- (2) Drive-in anneal (optional)

(B) Optional treatment for coverage structures (Fig. 2): Insert process steps after nitride breakthrough but before barrier/seed deposition. One mask required. Several process options (i) – (iv):

(i) Fig. 4 (a) – photoresist as doping mask
- (1) Pattern photoresist to leave openings over interconnects with vias underneath
- (2) Selectively deposit dopant layer
- (3) Remove photoresist using a Cu-inert chemical
- (4) Drive-in anneal

(ii) Fig. 4 (b) – photoresist as doping mask
- (1) Pattern photoresist to leave openings over interconnects with vias underneath
- (2) Ion-implant dopant
- (3) Remove photoresist using a Cu-inert chemical
- (4) Drive-in anneal

(iii) Fig. 4 (a) – SiN/SiC as doping mask
- (1) Deposit thin SiN/SiC layer
- (2) Pattern photoresist to leave openings over interconnects with vias underneath
- (3) Etch SiN/SiC, remove PR
- (4) Selectively deposit dopant layer
- (5) Drive-in anneal

(iv) Fig. 4 (b) – SiN/SiC as doping mask
- (1) Deposit thin SiN/SiC layer
- (2) Pattern photoresist to leave openings over interconnects with vias underneath
- (3) Etch SiN/SiC, remove PR
- (4) Ion-implant dopant
- (5) Drive-in anneal

Attorney's Docket No.: 42390.P12075 PATENT

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first, and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

Method of Making a Semiconductor Device
that has Copper Damascene Interconnects
with Enhanced Electromigration Reliability

the specification of which

_x_ is attached hereto.
_____ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign applications for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status—patented, pending, abandoned)

I hereby appoint Aloysius T. C. AuYeung, Reg. No. 3S,432; William Thomas Babbitt, Reg. No. 39,591; Kent D. Baker, Reg. No. 38,822; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Bravely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39 926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Thomas M. Coester, Reg. No P39,637; Roland B. Cortes, Reg. No. 39,152; William Donald Davis, Reg. No. 38,428; [Daniel M De Vos, Reg. No. 37,813; Karen L. Feistharnel, Reg. No. 40,264; David R. Halvorson, Reg. No. 33,395; Brian Don Hickman. Reg. No. 35,894; Eric Ho, Reg. No. P39,711; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139, Jeffrey D. Jacobs, Reg. No. 40,029; Dag H. Johansen, Reg.

No. 36,172; Stephen L. King, Reg. No. 19,180; Dolly M. Lee, Reg. No. 39,742; Michael J. Marie, Reg. No. 36,591; Kimberley G. Nobles, Reg. No. 38,255; Ronald W. Reagin, Reg. No. 20,340; James H Salter, Reg. No. 35,668, William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 3X,195; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 2S,128; Allan T. Sponseller, Reg. No. 38,318; Steven R. Sponseller, Reg. No. 39,384; David R. Stevens, Reg. No. 3B,626; Edwin H. Taylor, Reg. No. 25,129; Lester J. Vincent, Reg. No. 31,460; John Patrick Alard, Reg. No. 40,216; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys; and Gary B. Goates, Reg. No. 35,159; Michael Anthony DeSanctis, Reg. No. 39,957; Charles E. Shemwell, Reg. No. 40,171; Edwin A. Sloane, Reg. No. 34,728; and Judith A. Szepesi, Reg. No. 39,393; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 9002E, telephone (310) 207-3800, and Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468, Mark Seeley, Reg. No. 32,299; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; and Raymond J. Werner, Reg. No. 34,752 of INTEL CORPORATION with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Mark Seeley, c/o BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to Mark Seeley, (408) 765-7382.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Stefan Hau-Riege

Inventor's Signature X _____ Date X 11/17/01

Residence 1775 Milmont Drive #N205, Milpitas, CA 95035 Citizenship Germany
(City, State) (Country)

Post Office Address Same as above

Attorney's Docket No.: 42390.P12075

ASSIGNMENT
(For Execution Prior to Filing Patent Application)

PATENT

In consideration of good and valuable consideration, the receipt of which is hereby acknowledged, I the undersigned, Stefan Hau-Riege, hereby sell, assign, and transfer to Intel Corporation a corporation of Delaware, having a principal place of business at 2200 Mission College Boulevard, Santa Clara, California 95052, ("Assignee"), and its successors, assigns, and legal representatives, the entire right, title, and interest for the United States and all foreign countries, in and to any and all improvements that are disclosed in the application for the United States patent that has been executed by the undersigned prior hereto or concurrently herewith on the dates indicated below and is entitled "METHOD OF MAKING A SEMICONDUCTOR DEVICE THAT HAS COPPER DAMASCENE INTERCONNECTS WITH ENHANCED ELECTROMIGRATION RELIABILITY" and in and to said application and all divisional, continuing substitute, renewal, reissue, and all other patent applications that have been or shall be filed in the United States and all foreign countries on any of said improvements, and in and to all original and reissued patents that have been or shall be issued in the United States and all foreign countries on said improvements; and in and to all rights of priority resulting from the filing of said United States application; agree that said Assignee may apply for and receive a patent or patents for said improvements in its own name; and that, when requested, without charge to, but at the expense of, said Assignee, it successors, assigns, and legal representatives, to carry out in good faith the intent and purpose of this Assignment, the undersigned will execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all said improvements' execute all rightful oaths, assignments, powers of attorney, and other papers; communicate to said Assignee, its successors, assigns, and representatives all facts known to the undersigned relating to said improvements and the history thereof; and generally do everything possible that said Assignee, its successors, assigns, or representatives shall consider desirable for aiding in securing and maintaining proper patent protection for said improvements and for vesting title to said improvements, and all applications for patents and all patents on said improvements, in said Assignee, its successors, assigns, and legal representatives' and covenant with said Assignee, its successors, assigns, and legal representatives that no assignment, grant, mortgage, license, or other agreement affecting the rights and property herein conveyed has been made to others by the undersigned, and that full right to convey the same as herein expressed is possessed by the undersigned.

Each Inventor: Please also list the date that you signed the accompanying DECLARATION AND POWER OF ATTORNEY:

X 11/17/01, 2001
Date

X _____
Name:

X 11/17/01, 2001
Date

Attorney's Docket No.: 42390.P12075 PATENT

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first, and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

Method of Making a Semiconductor Device
that has Copper Damascene Interconnects
with Enhanced Electromigration Reliability

the specification of which

_x_ is attached hereto.

_____ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

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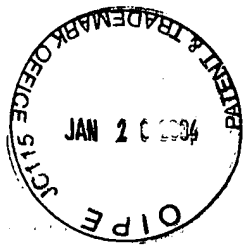

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(Application Number) Filing Date

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I hereby appoint Aloysius T. C. AuYeung, Reg. No. 3S,432; William Thomas Babbitt, Reg. No. 39,591; Kent D. Baker, Reg. No. 38,822; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Bravely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39 926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Thomas M. Coester, Reg. No P39,637; Roland B. Cortes, Reg. No. 39,152; William Donald Davis, Reg. No. 38,428; [Daniel M De Vos, Reg. No. 37,813; Karen L. Feisthamel, Reg. No. 40,264; David R. Halvorson, Reg. No. 33,395; Brian Don Hickman. Reg. No. 35,894; Eric Ho, Reg. No. P39,711; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139, Jeffrey D. Jacobs, Reg. No. 40,029; Dag H. Johansen, Reg.

No. 36,172; Stephen L. King, Reg. No. 19,180; Dolly M. Lee, Reg. No. 39,742; Michael J. Marie, Reg. No. 36,591; Kimberley G. Nobles, Reg. No. 38,255; Ronald W. Reagin, Reg. No. 20,340; James H Salter, Reg. No. 35,668, William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 3X,195; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 2S,128; Allan T. Sponseller, Reg. No. 38,318; Steven R. Sponseller, Reg. No. 39,384; David R. Stevens, Reg. No. 3B,626; Edwin H. Taylor, Reg. No. 25,129; Lester J. Vincent, Reg. No. 31,460; John Patrick Alard, Reg. No. 40,216; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys; and Gary B. Goates, Reg. No. 35,159; Michael Anthony DeSanctis, Reg. No. 39,957; Charles E. Shemwell, Reg. No. 40,171; Edwin A. Sloane, Reg. No. 34,728; and Judith A. Szepesi, Reg. No. 39,393; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 9002E, telephone (310) 207-3800, and Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468, Mark Seeley, Reg. No. 32,299; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; and Raymond J. Werner, Reg. No. 34,752 of INTEL CORPORATION with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Mark Seeley, c/o BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to Mark Seeley, (408) 765-7382.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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ASSIGNMENT

(For Execution Prior to Filing Patent Application)

PATENT

In consideration of good and valuable consideration, the receipt of which is hereby acknowledged, I the undersigned, R. Scott List, hereby sell, assign, and transfer to Intel Corporation a corporation of Delaware, having a principal place of business at 2200 Mission College Boulevard, Santa Clara, California 95052, ("Assignee"), and its successors, assigns, and legal representatives, the entire right, title, and interest for the United States and all foreign countries, in and to any and all improvements that are disclosed in the application for the United States patent that has been executed by the undersigned prior hereto or concurrently herewith on the dates indicated below and is entitled "METHOD OF MAKING A SEMICONDUCTOR DEVICE THAT HAS COPPER DAMASCENE INTERCONNECTS WITH ENHANCED ELECTROMIGRATION RELIABILITY" and in and to said application and all divisional, continuing substitute, renewal, reissue, and all other patent applications that have been or shall be filed in the United States and all foreign countries on any of said improvements, and in and to all original and reissued patents that have been or shall be issued in the United States and all foreign countries on said improvements; and in and to all rights of priority resulting from the filing of said United States application; agree that said Assignee may apply for and receive a patent or patents for said improvements in its own name; and that, when requested, without charge to, but at the expense of, said Assignee, it successors, assigns, and legal representatives, to carry out in good faith the intent and purpose of this Assignment, the undersigned will execute all divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all said improvements' execute all rightful oaths, assignments, powers of attorney, and other papers; communicate to said Assignee, its successors, assigns, and representatives all facts known to the undersigned relating to said improvements and the history thereof; and generally do everything possible that said Assignee, its successors, assigns, or representatives shall consider desirable for aiding in securing and maintaining proper patent protection for said improvements and for vesting title to said improvements, and all applications for patents and all patents on said improvements, in said Assignee, its successors, assigns, and legal representatives' and covenant with said Assignee, its successors, assigns, and legal representatives that no assignment, grant, mortgage, license, or other agreement affecting the rights and property herein conveyed has been made to others by the undersigned, and that full right to convey the same as herein expressed is possessed by the undersigned.

Each Inventor: Please also list the date that you signed the accompanying DECLARATION AND POWER OF ATTORNEY:

X 11/27, 2001	X N. Scott	X 11/27, 2001
Date	Name:	Date